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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,618	01/25/2001	Setsuo Nakajima	12732-007001	5724

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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,618	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-33* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1a and 1b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 13-33 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kuramasu et al. Patent Number 6,506,669.

5. Kuramasu discloses the semiconductor method substantially as claimed. See **FIGS 1-13** where Kuramasu teaches a method of manufacturing a semiconductor device comprising:

forming a heat absorbing layer **4** in an island form over a substrate;

forming an insulating film **3, 5** over said heat absorbing layer;

forming a non-single crystalline semiconductor film **15** on said insulating film;

irradiating said non-single crystalline semiconductor film with light so that said semiconductor film is melted and solidified; and

patterning said semiconductor film into a semiconductor island **2**, the semiconductor island not overlapping with the heat absorbing layer,

wherein a channel length direction of the semiconductor island is parallel to a longitudinal outer edge of said heat absorbing layer.

6. Pertaining to claim 14, Kuramasu teaches a method according to claim 13 wherein said semiconductor film is crystallized by said light.

7. Pertaining to claim 15, Kuramasu teaches a method according to claim 13 wherein said non-single crystalline semiconductor film is selected from an amorphous semiconductor film, a microcrystalline semiconductor film and a polycrystalline semiconductor film.

8. Pertaining to claim 16, Kuramasu teaches a method according to claim 13 wherein said semiconductor film comprises silicon.

9. Pertaining to claim 17, Kuramasu teaches a method according to claim 15 wherein a plurality of protrusions are formed on said semiconductor film after the irradiation, and a height of said protrusions is at least 30 nm.

10. Pertaining to claim 18, Kuramasu teaches a method according to claim 13 wherein said heat absorbing layer comprises a metal selected from the group consisting of Cr, Mo, Ti, Ta and W.

11. Pertaining to claim 19, Kuramasu teaches a method according to claim 13 wherein said absorbing layer functions as an electrode of a storage capacitance of a liquid crystal display device or an EL display device.

12. Pertaining to claim 20, Kuramasu teaches a method of manufacturing, a semiconductor device comprising:

forming a heat absorbing layer comprising a metal over a substrate;

forming a first insulating film over said heat absorbing layer;

forming a non-single crystalline semiconductor film on said first insulating film;

irradiating said non-single crystalline semiconductor film with light to crystallize said semiconductor film wherein said semiconductor film is melted at least partly and a plurality of protrusions are formed on the crystallize semiconductor film;

patterning the crystallized semiconductor film into at least one semiconductor island to form a channel region, the semiconductor island not overlapping with the heat absorbing layer;

forming a gate insulating film on the semiconductor island; and

forming a gate electrode on said gate insulating film,

wherein a longitudinal edge of said heat absorbing layer is approximately parallel to a channel length direction of said semiconductor island.

13. Pertaining to claim 21, Kuramasu teaches a method according to claim 20 wherein said heat absorbing, layer comprises a metal selected from the group consisting of Cr, Mo, Ti, Ta and W.

14. Pertaining to claim 22, Kuramasu teaches a method of manufacturing a semiconductor device comprising:

forming a heat absorbing layer comprising a metal over a substrate;

forming a first insulating film over said heat absorbing layer;

forming a non-single crystalline semiconductor film on said first insulating film;

irradiating said non-single crystalline semiconductor film with light to crystallize said semiconductor film wherein said semiconductor film is melted at least partly and a plurality of protrusions are formed on the crystallize semiconductor film;

patterning the crystallized semiconductor film into at least one semiconductor island having a channel region therein, the semiconductor island not overlapping with the heat absorbing layer;

forming a gate insulating film on the semiconductor island; and

forming a gate electrode on said gate insulating film, wherein a longitudinal edge of the beat absorbing layer is parallel to a channel length direction of the semiconductor island, and

wherein said protrusions are formed so that first regions of said channel region has a larger number of said protrusions and second regions of said channel region has no or a smaller number of said protrusions, and said first and second regions appear in turn in a direction orthogonal to the channel length direction of the semiconductor island.

15. Pertaining to claim 23, Kuramasu teaches a method according to claim 22 wherein said heat absorbing layer comprises a metal selected from the group consisting of Cr, Mo, TI, Ta and W.

16. Pertaining to claim 24, Kuramasu teaches a method according to claim 22 wherein said a height of said protrusions is at least 30 nm.

17. Pertaining to claim 25, Kuramasu teaches a method according to claim 22 further comprising a step of crystallizing said non-single crystalline semiconductor film before irradiating said light.

18. Pertaining to claim 26, Kuramasu teaches a method according to claim 22 wherein said light is a laser light.

19. Pertaining to claim 27, Kuramasu teaches a method according to claim 20 wherein said light is a laser light.

20. Pertaining to claim 28, Kuramasu teaches the method according to claim 20 wherein said semiconductor device is selected from a personal computer, a video camera, a portable information terminal, an electronic game equipment, and a digital camera.

21. Pertaining to claim 29, Kuramasu teaches the method according to claim 20 wherein said semiconductor device is a liquid crystal device.

22. Pertaining to claim 30, Kuramasu teaches the method according to claim 20 wherein said semiconductor device is an EL display device.

23. Pertaining to claim 31, Kuramasu teaches the method according to claim 22 wherein said semiconductor device is selected from a personal computer, a video camera, a portable information terminal, an electronic game equipment, and a digital camera.

24. Pertaining to claim 32, Kuramasu teaches the method according to claim 22 wherein said semiconductor device is a liquid crystal device

25. Pertaining to claim 33, Kuramasu teaches the method according to claim 22 wherein said semiconductor device is an EL display device.

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

30. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
April 6, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800